

Appl. No. 09/654,253
Amendment dated January 18, 2005
Reply to Final Office Action of November 17, 2005

Amendments to the Specification

Please replace the paragraph beginning at page 3, line 14 with the following rewritten paragraph:

Referring to FIG. 1, a simplified functional block diagram of a mismatch modeling tool 10 in an embodiment in accordance with the present invention is shown (the "mismatch tool 10" hereinafter). The mismatch tool 10 comprises the mismatch model $\sigma_{Id}^2 = \sum (\partial I_d / \partial p_j)^2 \sigma_{p_j}^2$ ("mismatch model 30" hereinafter); where I_d is drain current (for field effect devices and collector current for bipolar junction devices), and p_j is the j th physical process parameter. The mismatch model 30 predicts the statistical variance in the output current for any size transistor over terminal bias conditions. For field effect transistors, p_j may contain known parameters such as the threshold voltage, V_t , the flatband voltage, V_{fb} , the gate oxide thickness, T_{ox} , offsets in length, L , and width, W , geometries, mobility, μ_0 , dopant concentrations and resistances. Implicit in the mismatch model 30 is the local variation description which states that $\sigma_{p_j}^2$ scales inversely with geometry. The derivation and explanation of the mismatch model 30 is contained within the paper A Comprehensive MOSFET Mismatch Model by P. Drennan and C. Andrew, IEEE IEDM, 1999 ("Drennan et al." hereinafter), which the reader is referred to for additional detail regarding this particular mismatch model. Further explanation of the model is contained within Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design, - Ph. D. dissertation, Arizona State University, May 1999, by P. Drennan ("Drennan" hereinafter). For bipolar junction transistor, p_j may contain known parameters such as the ideal

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component of the base current, the pinched base sheet resistance, emitter and base resistances, and the space-charge-region recombination density.

Please replace the paragraph beginning at page 18, line 18, with the following rewritten paragraph:

Referring to FIG. 5, a mismatch results output frame for a current mirror scenario assumes a particular circuit. As an aide to the user, the message frame 158 will display that circuit. Thus – message frame 158 shows a picture of the assumed circuit 158a.